U.S. Patent Application
Attorney Docket No.: LKMP:104_US_

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **Richard Brosh et al.**

Examiner: **Shingleton, Michael B.**

U.S. Patent Application Serial No.: **09/998,714**

Group Art Unit: **2817**

For: **TRANSCONDUCTANCE POWER AMPLIFIER**

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BRIEF ON APPEAL
(37 C.F.R. §1.192)

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Honorable Sir:

Applicants respectfully appeal the decision of the Primary Examiner to finally reject Claims 1-5, as set forth in the final Office Action of May 21, 2003.

REAL PARTY IN INTEREST

The Real Party in Interest in this matter is BAE Systems Information and Electronics Integration, Inc., assignee.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences pertaining to this matter.

STATUS OF CLAIMS

Claims 1-5 are currently pending in this application. The Primary Examiner issued a Final Rejection of Claims 1-4 and objected to Claim 5 on May 27, 2003. Claims 1-5 are the subject of this appeal.

STATUS OF AMENDMENTS

An Amendment to the claims and a Request for Reconsideration was filed on February 20, 2003 in response to the first Office Action of November 20, 2002. This amendment was submitted and entered prior to the issuance of a Final Rejection.

SUMMARY OF THE INVENTION

The present invention relates to a transconductance power amplifier for amplifying a signal to a capacitive load, comprising:

only two N-channel MOSFET transistors, including;

a first N-channel enhancement MOSFET transistor operatively arranged to source current to said capacitive load, wherein said first N-channel MOSFET transistor has a threshold gate to source voltage;

a second N-channel enhancement MOSFET transistor operatively arranged to sink current to said capacitive load, said amplifier further comprising;

an operational amplifier operatively arranged to transmit and amplify an input signal to both of said first and second MOSFET transistors; and,

means for biasing said first N-channel enhancement MOSFET transistor such that its gate to source voltage is always at or above its threshold when the load draws near zero current so that very little additional gate charge is required to turn it on more fully.

ISSUES PRESENTED FOR REVIEW

1. Whether Claims 1-5 are non-obvious under 35 U.S.C. §103(a) to a person having ordinary skill in the art at the time the invention was made and therefore patentable over United States Patent No. 6,150,853 (Chrappan *et al.*) in view of United States Patent No. 5,378,938 (Birdsall *et al.*)?

GROUPING OF CLAIMS

Applicants respectfully submit that Claims 1-5 do not stand or fall together. Claims 1, 3 and 4 are independent claims. While Claims 2 and 5 are dependent claims, they too have independent patentable significance over and above the claims from which they depend.

ARGUMENT

1. The Rejection of Claim 3 under 35 U.S.C. §103(a)

a.) Summary of the Rejection:

The Examiner rejected Claim 3 under 35 U.S.C. §103(a) as being anticipated by Chrappan *et al.* (USPN 6,150,853).

b.) The Reference cited by The Examiner:

For purposes of providing background, Applicants briefly discuss the Chrappan *et al.* reference cited by the Examiner. Chrappan *et al.* describes an integrated circuit for driving at least one pair of discrete power field-effect transistors in Figs. 2 to 4 which overcomes limitations of the

prior art as featured in Fig. 1. As noted in Chrappan *et al.*, the prior art and Chrappan *et al.* require more than two MOSFET transistors.

> With reference to FIG. 1, class AB operation requires that a simultaneous ON condition of both the output power transistors M2 and M3, at a controlled current, be ensured during zero-crossing (i.e. when the current flowing through the load at the output node OUT is null). In the case of a pair of n-channel power transistors, this condition can be ensured (as already described in U.S. Pat. No. 5,216,381) by the use of diode-configured transistor M1, current generator I1, and operational amplifier OP2 to jointly perform a control function of the low-side (pull-down) power transistor M3.
>
> Of course, the circuit arrangement of the invention is applicable also in the case of a circuit that employs a pair of p-channel field effect output transistors, by inverting the sign of the voltages and the sense of the currents. In this case, as will be evident to a skilled person, it will be the pull-down or lower transistor M4 of the output pair, to have its gate driven by a level shifting buffer BF1 and therefore connected, through the same buffer BF1, to the gate of the integrated transistor M2 of the limiting network. Such an alternative embodiment is depicted in FIG. 3. (See Col. 6, lines 48-54)

Thus, Chrappan *et al.* teaches a circuit with at least THREE MOSFET transistors.

c.) The Present Invention :

Some of the key structural elements of the present invention are described in Claim 3. Claim 3 teaches a transconductance power amplifier for amplifying a signal to a capacitive load, comprising:

only two N-channel MOSFET transistors, including;

a first N-channel enhancement MOSFET transistor operatively arranged to source current to said capacitive load;

a second N-channel enhancement MOSFET transistor operatively arranged to sink current to said capacitive load, said amplifier further comprising;

an operational amplifier operatively arranged to transmit and amplify an input signal to both of said first and second MOSFET transistors; and,

means for reducing current to said first N-channel enhancement MOSFET transistor when said power amplifier sinks current from the load through said second N-channel enhancement MOSFET transistor.

d.) Arguments:

i.) The combination/modification propounded by the Primary Examiner does not teach or suggest all of the claim limitations of the present invention.

"To establish a *prima facia* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one having ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or the references when combined) must teach or suggest **all** the claim limitations." MPEP §2142, citing, *In re Vaeck*, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991).

The Primary Examiner indicates that diodes and diode-connected transistors are recognized equivalents. However, even if such an equivalent is recognized, Chrappan *et al.* cannot cure the lack of teachings regarding **TWO** MOSFETs and **ONE** operational amplifier. Thus, the Primary Examiner has failed to establish a *prima facia* case for obviousness for the rejection of Claim 3 because neither Chrappan *et al.* alone or in combination with equivalents known to those of skill in the art, arrives at **all** the limitations of the claim.

ii.) The reference cited by the Primary Examiner teaches away from the present invention.

In addition to failing to teach all of the limitations of Claim 3, Chrappan *et al.* teaches away from the present invention, requiring more than two MOSFET transistors and more than one operational amplifier. This creates inefficiency, hinders stability and accuracy, and adds to the cost of circuit design and production. Finally, there is no motivation, teaching or suggestion for one skilled in the art to modify the Chrappan *et al.* circuit to arrive at all of the features of Claim 3.

2. The Rejection of Claims 1-5 under 35 U.S.C. §103(a)

a.) Summary of the Rejection:

The Primary Examiner rejected Claims 1-5under 35 U.S.C. §103(a) as being obvious and unpatentable over Chrappan *et al.* (USPN 6,150,853) alone and in combination with Birdsall *et al.* (USPN 5,378,938).

b.) The References cited by The Examiner:

Chrappan *et al.* was discussed above. Also as noted in Chrappan *et al.*, the prior art and Chrappan *et al.* require more than one operational amplifier. "The operational amplifier OP1 represents a signal amplifying stage which is responsible of (sic) the system's gain." (Col. 5, lines 22-23). "The diode M1 permits to obtain at the drain terminal thereof a voltage, which is compared with the gate voltage of the upper (pull-up) power transistor M2 by the operational amplifier OP2, which controls the gate of the lower power transistor M3." (Col. 5, lines 33-35). **Thus, Chrappan *et al.* teaches a circuit with at least TWO operational amplifiers.**

Birdsall *et al.* describes a sample-and-hold circuit which makes NO mention of a MOSFET transistor. The word "MOSFET" **cannot be found anywhere** in the Birdsall *et al.* reference either explicitly or implicitly.

c.) The Present Invention:

Elements of the present invention have been discussed above as relating to independent Claim 3. Claim 1 teaches a transconductance power amplifier for amplifying a signal to a capacitive load, comprising:

only two N-channel MOSFET transistors, including;

a first N-channel enhancement MOSFET transistor operatively arranged to source current to said capacitive load, wherein said first N-channel MOSFET transistor has a threshold gate to source voltage;

a second N-channel enhancement MOSFET transistor operatively arranged to sink current to said capacitive load, said amplifier further comprising;

an operational amplifier operatively arranged to transmit and amplify an input signal to both of said first and second MOSFET transistors; and,

means for biasing said first N-channel enhancement MOSFET transistor such that its gate to source voltage is always at or above its threshold when the load draws near zero current so that very little additional gate charge is required to turn it on more fully.

Claim 4 teaches a transconductance power amplifier for amplifying a signal to a capacitive

load, comprising:

a maximum of five (5) active components, including;

a first N-channel enhancement MOSFET transistor operatively arranged to source current to said capacitive load, wherein said first N-channel MOSFET transistor has a threshold gate to source voltage;

a second N-channel enhancement MOSFET transistor operatively arranged to sink current to said capacitive load, said amplifier further comprising;

an operational amplifier arranged to transmit and amplify an input signal to both of said first and second MOSFET transistors; and,

means for biasing said first N-channel enhancement MOSFET transistor such that its gate to source voltage is always at or above its threshold when the load draws near zero current so that very little additional gate charge is required to turn it on more fully. Claim 2 depends from independent Claim 1 while Claim 5 depends from independent Claim 4. However, each of these dependent claims has independent patentable significance over and above the claims from which they depend. For example, Claim 2 further comprises a means for reducing current to the first N-channel enhancement MOSFET transistor when the power amplifier sinks current from the load through the second N-channel enhancement MOSFET transistor. Claim 5 adds the limitations of "wherein said power amplifier comprises a single operational amplifier, only two MOSFET transistors, and only two bipolar transistors".

d.) Arguments:

i.) The combination/modification propounded by the Primary Examiner does not teach or suggest all of the claim limitations of the present invention.

As noted above, a *prima facia* case for obviousness requires that the prior art reference must teach or suggest all the claim limitations. All of the pending Claim 1-5 have numerous features not taught by Chrappan *et al.* Specifically, Claims 1-3 require only two MOSFETs and one operational amplifier. Claims 4 and 5 require at least five active components. None of these features can be found in Chrappan *et al.* or in Birdsall *et al.* Combining these references also does not arrive at all of the limitations of the present invention. Specifically, Birdsall's teaching of one operational amplifier in Fig. 3 does not compensate for the lack of Chrappan's teachings of only two MOSFET transistors. Thus, the Primary Examiner has failed to establish a *prima facia* case for obviousness for the rejection of Claims 1-5 because neither Chrappan *et al.* alone or in combination with the teachings of Birdsall *et al.*, arrives at **all** the limitations of these claims.

ii.) The reference cited by the Primary Examiner considered individually or collectively with information known to one of ordinary skill in the art, does not contain sufficient teaching, suggestion or motivation to combine/modify the references to create the present invention.

"Virtually all inventions are combinations of old elements. Therefore, an Examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue." *In re Rouffet*, 47 U.S.P.Q.2d 453 (Fed. Cir. 1998).

When a rejection depends on a combination of prior art references, there must be some

teaching, suggestion, or motivation to combine the references and the teachings of the references can be combined only if there is some suggestion or incentive to do so. *In Re Lee*, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002), citing *In re Fine*. Hence, elements of separate patents cannot be combined when there is no suggestion of such combination in those patents. *Panduit Corp. v. Dennison Manufacturing Co.*, 1 U.S.P.Q.2d 1593 (Fed. Cir. 1987). Additionally, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills* 16 U.S.P.Q.2d 1430.

In the present case, none of the prior art references cited by the Primary Examiner contain an explicit or implicit teaching, suggestion, or motivation to create the subject invention and none teach, suggest, or motivate one to combine/modify their respective teachings with others to create the subject invention. Specifically, there is no teaching, suggestion or motivation for modifying the at least three MOSFET, two operational amplifier teachings of Chrappan *et al.* with the zero MOSFET teachings of Birdsall *et al.* to arrive at the limitations of the present invention.

iii.) The references cited by the Primary Examiner teaches away from the present invention.

Furthermore, as previously stated, Chrappan *et al.* teaches away from the invention as limited by the elements in Claims 1-5. This is also certainly the case with the Birdsall *et al.* reference which makes NO mention of any MOSFET transisitors. The Primary Examiner must also explain the reasons one of ordinary skill in the art would have been motivated to select the references and combine them to render the claimed invention obvious. *In Re Lee*, 61 U.S.P.Q.2d 1430 (Fed. Cir.

2002); *In re Rouffet*, 47 U.S.P.Q.2d 1453, Applicant respectfully submits that one having skill in the art would not have been led, or motivated, to select the references for combination as suggested by the Examiner. As indicated *supra*, none of the references cited teaches a circuit having only two MOSFET transistors. Hence, one having skill in the art of circuit design would readily appreciate that the a circuit with at least three MOSFET transistors or one with NO MOSFET transistors is very different and incompatible with a circuit having only two MOSFET transistors.

Conclusion

For the reasons set forth above, Applicants respectfully submit that Claims 1 through 5 are patentable over Chrappan *et al.* and Birdsall *et al.* Accordingly, Applicants pray that this Honorable Board will reverse the Primary Examiner's rejection of Claims 1-5.

Respectfully submitted,

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SCG

Appendix

Reprinted here below are the claims involved in this appeal:

1. A transconductance power amplifier for amplifying a signal to a capacitive load, comprising:

only two N-channel MOSFET transistors, including;

a first N-channel enhancement MOSFET transistor operatively arranged to source current to said capacitive load, wherein said first N-channel MOSFET transistor has a threshold gate to source voltage;

a second N-channel enhancement MOSFET transistor operatively arranged to sink current to said capacitive load, said amplifier further comprising;

an operational amplifier operatively arranged to transmit and amplify an input signal to both of said first and second MOSFET transistors; and,

means for biasing said first N-channel enhancement MOSFET transistor such that its gate to source voltage is always at or above its threshold when the load draws near zero current so that very little additional gate charge is required to turn it on more fully.

2. The transconductance power amplifier for amplifying a signal to a capacitive load recited in Claim 1 further comprising means for reducing current to said first N-channel enhancement MOSFET transistor when said power amplifier sinks current from the load through said second N-channel enhancement MOSFET transistor.

3. A transconductance power amplifier for amplifying a signal to a capacitive load, comprising:

only two N-channel MOSFET transistors, including;

a first N-channel enhancement MOSFET transistor operatively arranged to source current to said capacitive load;

a second N-channel enhancement MOSFET transistor operatively arranged to sink current to said capacitive load, said amplifier further comprising;

an operational amplifier operatively arranged to transmit and amplify an input signal to both of said first and second MOSFET transistors; and,

means for reducing current to said first N-channel enhancement MOSFET transistor when said power amplifier sinks current from the load through said second N-channel enhancement MOSFET transistor.

4. A transconductance power amplifier for amplifying a signal to a capacitive load, comprising:

a maximum of five (5) active components, including;

a first N-channel enhancement MOSFET transistor operatively arranged to source current to said capacitive load, wherein said first N-channel MOSFET transistor has a threshold gate to source voltage;

a second N-channel enhancement MOSFET transistor operatively arranged to sink current to said capacitive load, said amplifier further comprising;

an operational amplifier arranged to transmit and amplify an input signal to both of said first

and second MOSFET transistors; and,

means for biasing said first N-channel enhancement MOSFET transistor such that its gate to source voltage is always at or above its threshold when the load draws near zero current so that very little additional gate charge is required to turn it on more fully.

5. The transconductance power amplifier recited in Claim 4 wherein said power amplifier comprises a single operational amplifier, only two MOSFET transistors, and only two bipolar transistors.